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10EC666

Sixth Semester B.E. Degree Examination, Aug./Sept.2020
Digital System Design using Verilog

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. What is meant by Design methodology? Explain the basic steps of design methodology with the help of flow chart. **(10 Marks)**

b. Suppose a factory has two vats, only one of which is used at a time. The liquid in the vat in use needs to be at the right temperature, between 25°C and 30°C. Each vat has two temperatures sensors indicating whether the temperature is above 25°C and above 30°C, respectively. The vats also have low level sensors. The supervisor needs to be wokenup by a buzzer when the temperature is too high or too low or the vat level is too low. He has a switch to select which vat is in use. Design a circuit of gates to activate the buzzer as required. **(05 Marks)**

c. Explain static load levels imposed in real world circuit. **(05 Marks)**

2 a. Develop a verilog code of a encoder for use in a domestic burglar alarm that has sensors for each of eight zones. Sensor is '1' when an intrusion is detected in that zone and '0' otherwise. The encoder has three bits of output, encoding the zones as follows: Zone1 : 000, Zone2 : 001, Zone3 : 010, Zone4 : 011, Zone5 : 100, Zone6 : 101, Zone7 : 110, Zone8 :111. **(08 Marks)**

b. Draw the circuit diagram of parity tree for generating and checking even parity for 8 bit code. **(04 Marks)**

c. Implementing the Boolean function $F = (x + y\bar{z})(\overline{yz})$ using sum-of-product form. Use laws of Boolean Algebra for reduction. **(08 Marks)**

3 a. Write a note on the various operations that can be performed on fixed-point members. **(10 Marks)**

b. Develop a verilog model of a code converter to convert the 4-bit unsigned binary integer to Gray code. **(10 Marks)**

4 a. Explain the asynchronous timing methodology in detail. **(08 Marks)**

b. Design and develop a verilog code for mod 10 counter. **(06 Marks)**

c. Develop a verilog model for an interval timer that has clock, load and data input parts and a terminal-count output port. The timer must be able to count intervals of upto 1000 clock cycles. **(06 Marks)**

PART – B

5 a. Develop a verilog model of a dual port 4k × 16-bit flow through SSRAM. One port allows data to be written and read, while other port only allows data to be read. **(08 Marks)**

b. What is the benefit of allowing PLD in a system to be reprogrammed? Explain. **(06 Marks)**

c. Compute the 12-bit ECC word corresponding to the 8-bit data word 01100001. **(06 Marks)**

6 a. Write a Gumnet assembly language program to find greater of two valves. **(10 Marks)**

b. Explain Arithmetic, Logical, Shift and Memory instructions. **(10 Marks)**

7 a. Discuss the modelling tristate drivers in verilog. (08 Marks)
b. Explain the mechanism for input / output controllers to request on interrupt. (08 Marks)
c. Explain the working of successive approximation ADC. (04 Marks)

8 a. Briefly explain Design optimization. (10 Marks)
b. Explain Build In Self Test (BIST) techniques. (10 Marks)

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